AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor integrated circuit device, comprising:

a latch ~~provided on the~~circuit coupled to an output of a memory circuit or ~~on the~~an input of a logic circuit,

wherein said latch circuit includes a signal selector for switching between a feedback signal of normal operation mode and a test signal of test operation mode in compliance with ~~the~~an operation mode signal to send out to a feedback loop.

2. (currently amended) A semiconductor integrated circuit device according to claim 1, wherein:

said latch circuit is ~~provided at the~~coupled to the output of said memory circuit and,

said signal selector is controlled by said operation mode signal for sending out to said feedback loop either ~~one of the~~a latch output signal as the feedback signal or ~~the~~an input signal to said memory as the test signal.

3. (currently amended) A semiconductor integrated circuit device according to claim 1, wherein:

said latch circuit is ~~provided at~~coupled to the output of said memory circuit,

said signal selector includes a logic gate for receiving said operation mode signal and latch output signal, and

said logic gate outputs fixedly an output signal of a predetermined level by the operation mode signal in the test ~~mode~~ operation mode for sending out to a feedback loop as said test signal.

4. (currently amended) A semiconductor integrated circuit device according to claim 1, wherein:

said latch circuit is provided at the output of ~~said~~a memory circuit;

said latch circuit has a first switch for sending ~~the~~a read-out signal from a memory cell in said memory to an input terminal of a first inverter under the control of a switch control signal, a second inverter for receiving ~~the~~an output signal of said first inverter on ~~the~~an input terminal, and a second switch for sending ~~the~~an output

signal of said second inverter to the input terminal of said first inverter under the control of said switch control signal, and said latch outputs a latch circuit output signal from ~~the~~an output terminal of said second inverter;

said signal selector has a third switch for sending ~~the~~an input signal fed to said memory to the input terminal of said first inverter as the test signal under the switching control of said switch control signal, and a signal generator for generating said switch control signal; and

said signal generator turns off said third switch in the normal operation mode by using said operation mode signal to perform a complementary switching control of said first and second switches by using clock pulses as said switch control signal, and turns off said first and second switches and turns on said third switch in the test operation by said operation mode signal.

5. (currently amended) A semiconductor integrated circuit device according to claim 1, wherein:

said latch circuit is ~~provided at~~coupled to the input of ~~said~~a logic circuit;

said latch circuit includes a first latch for receiving ~~thean~~ input signal in the normal operation mode and a second latch for generating ~~thea~~ signal input to said logic circuit upon reception of ~~thean~~ output from said first latch; and

said signal selector is provided in ~~thea~~ feedback loop of said first latch.

6. (currently amended) A semiconductor integrated circuit device according to claim 5, wherein:

said first latch has a first switch for sending said input signal to ~~thean~~ input terminal of a first inverter under the ~~switching~~control of a switch control signal, a first clocked inverter for receiving ~~thean~~ output signal from said first inverter on ~~thean~~ input terminal under the control of clock pulses, and a second switch for sending ~~thean~~ output signal from said first clocked inverter to the input terminal of said first inverter under the control of said ~~switching~~switch control signal;

said second latch has a circuit under the control of said clock pulses for performing signal collection and signal retention ~~in~~ complementary to said first latch, a second inverter for generating an output signal to ~~thean~~

input of said logic circuit, and a third inverter for generating an output signal for test scan;

said signal selector has a second clocked inverter under the control of said switch control signal for receiving ~~thea~~ test input signal on ~~thean~~ input terminal, a third switch for sending ~~thean~~ output signal from said second clocked inverter to ~~thean~~ input of said second switch under the switching control of said clock pulses, and a signal generator for generating said ~~switching~~switch control signal;

wherein said signal generator turns off said second clocked inverter by said operation mode signal during the normal operation mode, passing said clock pulses to said first and second switches as said switch control signal, in order to perform the complementary operation of signal collection and signal retention in response to the input signal by the first and second latches; and

wherein said signal generator turns off said first switch and turns on said second switch during the test mode in accordance with said operation mode signal, in order to perform the complementary operation of signal collection and signal retention by the first and second latches in response to the test input signal passing through said

second clocked inverter in the normal operation mode.

7. A semiconductor integrated circuit device, comprising a circuit, said circuit operating in either

a first mode for operating as ~~said~~a latch; or

a second mode for passing through ~~the~~a signal input from a signal switching circuit provided in ~~the~~a feedback loop of said latch.

8. (currently amended) A semiconductor integrated circuit device according to claim 7, wherein:

said first mode is ~~the~~a normal operation mode, and

said second mode is ~~the~~a test mode.

9. (original) A semiconductor integrated circuit device, comprising:

a first input node;

a transfer gate coupled to said first input node;

an output node coupled to said transfer gate;

a feedback loop provided between said first transfer gate and said output node; and

a second input node coupled to said feedback loop;

said first transfer gate in a first mode transferring

data input from said input node to said output node based on clock signals, said first transfer gate in a second mode disconnecting said input node from said output node; and

data being input to said second input node in said second mode.

10. (currently amended) A semiconductor integrated circuit device according to claim 9, wherein:

said semiconductor integrated circuit device further comprises a ~~multiplexor~~multiplexer provided in said feedback loop,

said ~~multiplexor~~multiplexer being coupled to said output node and said second input node to select said output node in said first mode and to select said second input node in said second mode.

11. (original) A semiconductor integrated circuit device according to claim 9, wherein:

said semiconductor integrated circuit device further comprises a second transfer gate provided in said feedback loop,

said second transfer gate determining whether or not to feed back the data transferred to said output node based

on said clock signal in said first mode, and transferring to said output node the data input to said second input node in said second mode.